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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/893,976	06/29/2001	Ik Soo kim	8733.437.00	6152

30827 7590 11/05/2004

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EXAMINER
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KIELIN, ERIK J

ART UNIT	PAPER NUMBER
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2813

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/893,976

Applicant(s)

KIM, IK SOO

Examiner

Erik Kielin

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 18 August 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1,3-7,9-11 and 13-24 is/are pending in the application.
- 4a) Of the above claim(s) 21 and 22 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3-7,9-11,13-20,23 and 24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

### DETAILED ACTION

This action responds to the Amendment filed 18 August 2004.

#### *Claim Status*

New claim: 24  
Withdrawn claims: **21, 22**  
Canceled claims: 2, 8 and 12  
Active claims: **1, 3-7, 9, 10, and 11, 13-20, 23, and 24**

#### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim **23** is rejected under 35 U.S.C. 102(b) as being anticipated by Applicant's admitted prior art (**APA**).

**APA** discloses a liquid crystal display device and method of manufacturing the device comprising forming each of the following:

- a gate electrode **6** on a substrate **1**;
- a gate insulating film **12** on the substrate **1** and over the gate electrode **6**;
- a semiconductor layer **14** on the gate insulating film **12** and over the gate electrode **6**;
- a source electrode **8** and a drain electrode **10** on the semiconductor layer **14** and adjacent the gate electrode **6**, wherein the source and drain electrodes oppose each other, each of the source electrode and drain electrode including at least one protrusion that extends toward the opposing electrode and the protrusion of the source electrode is offset from the protrusion of the

drain electrode (**note:** the adjacent edges of the source and drain electrodes form “at least one protrusion,” as shown in prior art Fig. 3C --especially in the cross-section-- and that the protrusions are necessarily “offset” in order to form the channel);

a protective layer **18** on the gate insulating film **12** and over the source and drain electrodes **8, 10**; and

a pixel electrode **22** on the protective layer **18**. (See instant specification, paragraphs [0003]-[0013] and Figs. 1 through 3E.)

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims **1, 3-7, 9, 10 and 11, 13-20 and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (APA) in view of JP 2-58030 A (Taniguchi et al.).

Regarding claims **1, 11 and 24**, APA discloses a liquid crystal display device and method of manufacturing the device comprising forming each of the following:

a gate electrode **6** on a substrate **1**;

a gate insulating film **12** on the substrate **1** and over the gate electrode **6**;

a semiconductor layer **14** on the gate insulating film **12** and over the gate electrode **6**;

a source electrode **8** and a drain electrode **10** on the semiconductor layer **14** and adjacent the gate electrode **6**, wherein the source and drain electrodes oppose each other and each includes at least one protrusion that extends toward the opposing electrode (the adjacent edges of the source and drain electrodes are form one protrusion, as shown in Fig. 3C --especially in the cross-section) and the protrusion extends directly from a data line and wherein an entire area of the channel is formed over the gate electrode;

a protective layer **18** on the gate insulating film **12** and over the source and drain electrodes **8, 10**;

a pixel electrode **22** on the protective layer **18**; and

wherein the gate electrode **6** underlies a part of the data line **4**, the source electrode **8** and the drain electrode **10** and a part of the drain electrode so that the channel is formed at parts of the source and drain electrodes facing the protrusion, **the entirety of the protrusions of the source and drain electrodes is formed within the area of the semiconductor layer**, and the protrusion of the source electrode is **offset** from the protrusion of the drain electrode, as shown in prior art Fig. 3C cross-section view. (Note: the adjacent edges of the source and drain electrodes form “at least one protrusion,” as shown in prior art Fig. 3C --especially in the cross-section-- and that the protrusions are necessarily “offset” in order to form the channel.)

(See instant specification, paragraphs [0003]-[0013] and Figs. 1 through 3E.)

**APA** does not teach that the channel has and “Z”-shape (instant claims 1 and 11) or that the source and drain electrodes have a plurality of protrusions (instant claim 24).

**Taniguchi** teaches a liquid crystal display and method of manufacturing the display wherein the source electrode **SD2** and the drain electrode **SD1** each include plural protrusions **d1**

that extend toward the opposing electrode in order to beneficially increase the channel width of the transistor, thereby creating a "Z"-shaped channel having an entire area of the channel formed over the gate electrode. (See Abstract and Figs. 1 and 2.)

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use the source/drain electrodes having plural protrusions and the consequent "Z"-shaped channel having the protrusions formed entirely over the area of the semiconductor layer in the APA TFT, in order to beneficially increase the channel width of the transistor, which enables reduction of the TFT size and improves the aperture rate, as taught by **Taniguchi** (Abstract). Note, because APA forms the entire source/drain electrodes over the semiconductor layer, and because **Taniguchi** forms plural protrusions over the semiconductor layer to increase the channel width, one of ordinary skill would recognize that the entirety of the protrusions formed in **Taniguchi** should be formed entirely over the semiconductor layer in order to further increase the channel width, as taught to be beneficial by **Taniguchi**. Further in this regard, nowhere in the instant specification is the feature that the protrusions are formed entirely over the area of the semiconductor layer, discussed or taught to be critical to the instant invention. Therefore it is not considered to have critical value in light of the applied art --especially given that **Taniguchi** teaches the same benefit as does the instant specification of increased channel width and decreased TFT size. In other words it is not novel or non-obvious to form the source/drain electrode protrusions entirely over the semiconductor layer, given the art of record teachings showing (1) the source/drain electrodes formed entirely over the semiconductor layer (APA) and (2) the plural protrusions used beneficially to increase channel width (**Taniguchi**).

Regarding claims 3 and 13, **APA** discloses the active layer **14** on the gate insulating film **12**; and the ohmic contact layer **16** on the active layer **14**.

Regarding claims 4 and 14, **APA** teaches that the ohmic contact layer **16** contains an opening corresponding to the channel **24** (Fig. 3C; paragraph [0009] --especially the last two sentences), but does not teach that the channel is "Z"-shaped.

**Taniguchi** shows that the channel is "Z"-shaped.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use a "Z"-shaped channel as the channel of **APA** to increase the channel width as taught by **Taniguchi**.

Regarding claims 5, 6, 15, and 16, **APA** discloses that the active layer is undoped silicon and the ohmic contact layer is doped silicon (instant specification, p. 4, paragraph [0008]).

Regarding claims 7 and 17, the **APA** discloses that standard channel width is about 25  $\mu\text{m}$  (instant specification, p. 3, paragraph [0005]), but does not teach a channel width of greater than 50  $\mu\text{m}$ .

**Tanaguchi** does not indicate the width of the channel but indicates that the width should be increased. Also the **Tanaguchi** Fig. 1 shows that the channel width is more than doubled by comparing a source/drain electrodes without protrusions to those source/drain electrodes **SD2**, **SD1**, with protrusions **d1** the same manner as presently proposed in the instant invention.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to width the channel width of **APA** to greater than 50  $\mu\text{m}$  by forming the protruding portions of the source/drain electrodes of **Tanaguchi** on those source/drain electrodes of **APA** because **Tanaguchi** teaches that the channel width should be longer than in the absence of such

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protrusions and shows geometrically that the width of the channel is more than doubled.

Moreover, these claims are *prima facie* obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. *In re Woodruff*, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also *In re Huang*, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also *In re Boesch*, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious). In the instant case, the result of forming the protrusions on the source/drain electrodes expectedly increases the channel width as clearly taught by **Tanaguchi**.

Regarding claim 18, **APA** discloses that the channel extends only over the gate electrode 6.

Regarding claims 9 and 19, **APA** discloses that the pixel electrode 22 contacts the drain electrode 10 through an opening 20 in the protective layer 18 (Fig. 3E).

Regarding claims 10 and 20, **APA** discloses that the data line 4 is in electrical communication with the source electrode 8 (Fig. 3E).

### ***Response to Arguments***

5. Applicant's arguments filed 18 August 2004 have been fully considered but they are not persuasive.



Applicant argues that the **APA** fails to teach various features. Examiner respectfully disagrees. In particular, the adjacent edges of the source and drain electrodes form “at least one protrusion,” as shown in prior art Fig. 3C --especially in the cross-section-- and that the protrusions are necessarily “offset” in order to form the channel. Examiner respectfully submits that the claims fail to provide sufficient description of the protrusions and the nature of the offsetting of the source/drain electrodes to distinguish over the **APA**.

Applicant argues that **APA** in view of **Taniguchi** fails to teach various features. Examiner respectfully disagrees. In particular, because **APA** forms the entire source/drain electrodes over the semiconductor layer, and because **Taniguchi** forms plural protrusions over the semiconductor layer to increase the channel width, one of ordinary skill would recognize that the entirety of the protrusions formed in **Taniguchi** should be formed entirely over the semiconductor layer in order to further increase the channel width, as taught to be beneficial by **Taniguchi**. Further in this regard, nowhere in the instant specification is the feature that the protrusions are formed entirely over the area of the semiconductor layer, discussed or taught to be critical to the instant invention. Therefore it is not considered to have critical value in light of the applied art --especially given that **Taniguchi** teaches the same benefit as does the instant specification of increased channel width and decreased TFT size. In other words it is not novel or non-obvious to form the source/drain electrode protrusions entirely over the semiconductor layer, given the art of record teachings showing (1) the source/drain electrodes formed entirely over the semiconductor layer (**APA**) and (2) the plural protrusions used beneficially to increase channel width (**Taniguchi**).

***Conclusion***

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

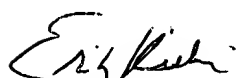
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached on 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Erik Kielin  
Primary Examiner  
3 November 2004